CLAIMS

What is claimed is:

1. Method of transferring ownership of a cache line between processors in a shared memory multi-processor computer system, comprising

sending a request transaction for ownership of a cache line from a first processor to a memory unit,

determining from the memory unit which one of a plurality of processors other than the first processor has ownership of the requested cache line and sending a recall transaction to a second processor, and

sending the requested cache line with ownership from the second processor to the first processor in response to the recall transaction.

2. Method according to claim 1, further comprising sending a response transaction from the first processor to the memory unit to confirm receipt of the requested cache line by the first processor.

3. Method according to claim 1, further comprising sending a response transaction from the second processor to the memory unit to confirm that the second processor has sent the requested cache line to the first processor.

4. Method according to claim 1, wherein the response transaction from the second processor to the memory unit includes a copy of the data on the requested cache line.

5. Method according to claim 1, wherein the response transaction from the second processor to the memory unit includes a copy of the data for the requested cache line only when the request for ownership of the cache line from the first processor does not include a guarantee that the first processor will make the requested cache line data available in response to a subsequent request for ownership of the cache line from a third processor.

6. Method according to claim 1, further comprising updating a tag in the memory unit to reflect transfer of ownership of the cache line to the first processor.

7. Method according to claim 1, wherein the computer system uses a directory-based cache coherency scheme.

8. Method of transferring a cache line between processors in a shared memory multi-processor computer system that uses a directory-based cache coherency scheme, comprising

sending a request transaction for ownership of a cache line from a first processor in an m^{th} cell to a memory unit in an n^{th} cell,

determining from the memory unit which one of a plurality of other processors in at least one p^{th} cell remote from the m^{th} and n^{th} cells has ownership of the requested cache line and sending a recall transaction to the processor with ownership,

sending the requested cache line with ownership from the other processor to the first processor in response to the recall transaction, and

sending a response transaction from the first processor to the memory unit to confirm receipt of the requested cache line by the first processor.

9. Method according to claim 8, wherein m = n = p.

10. Method according to claim 8, wherein m = n.

11. Method according to claim 8, wherein m = p.

12. Method according to claim 8, wherein n = p.

13. Method according to claim 8, further comprising sending a response transaction from the processor with ownership to the memory unit to confirm that the processor with ownership has sent the requested cache line to the first processor.

14. Method according to claim 8, wherein the response transaction from the processor with ownership to the memory unit includes a copy of the data for the requested cache line.

15. Method according to claim 8, wherein the response transaction from the processor with ownership to the memory unit includes a copy of the data for the requested

cache line only when the request for ownership of the cache line from the first processor does not include a guarantee that the first processor will make the requested cache line data available in response to a subsequent request for ownership of the cache line from a third processor.

16. Method according to claim 8, further comprising updating a tag in the memory unit to reflect transfer of ownership of the cache line to the first processor.

17. Method of transferring ownership of a cache line between processors in a shared memory multi-processor computer system that uses a directory-based cache coherency scheme, comprising

sending a request transaction for ownership of a cache line from a first processor to a memory unit,

determining from the memory unit which one of a plurality of processors other than the first processor has ownership of the requested cache line and sending a recall transaction to the processor with ownership,

sending the requested cache line with ownership from the processor with ownership to the first processor in response to the recall transaction,

sending a response transaction including a copy of the data for the requested cache line from the processor with ownership to the memory unit to confirm that the processor with ownership has sent the requested cache line to the first processor,

sending a response transaction from the first processor to the memory unit to confirm receipt of the requested cache line by the first processor, and

updating a tag in the memory unit to reflect transfer of ownership of the cache line to the first processor.

18. Apparatus for transferring ownership of a cache line between a plurality of processors in a multi-processor computer system with a shared memory unit, comprising

a first transaction line for providing a request transaction for ownership of a cache line from a first processor to the shared memory unit,

a second transaction line for providing a recall transaction to a second processor after determining from the shared memory unit which one of the plurality of processors other than the first processor has ownership of the requested cache line,

a third transaction line for providing transfer of the requested cache line from the second processor to the first processor in response to the recall transaction, and

a fourth transaction line for providing a response transaction from the first processor to the shared memory unit to confirm receipt of ownership of the requested cache line by the first processor.

19. Apparatus according to claim 18, further comprising a fifth transaction line for providing a response transaction from the second processor to the memory unit to confirm transfer of the requested cache line from the second processor to the first processor.

20. Apparatus according to claim 18, further comprising a fifth transaction line for providing a response transaction from the second processor to the memory unit to confirm transfer of the requested cache line from the second processor to the first processor together with a copy of the requested cache line data.

21. Apparatus according to claim 18, wherein the computer system uses a directory-based cache coherency scheme.